

International Symposium on Microarchitecture (MICRO)

Real-world Processing-in-Memory Systems for Modern Workloads

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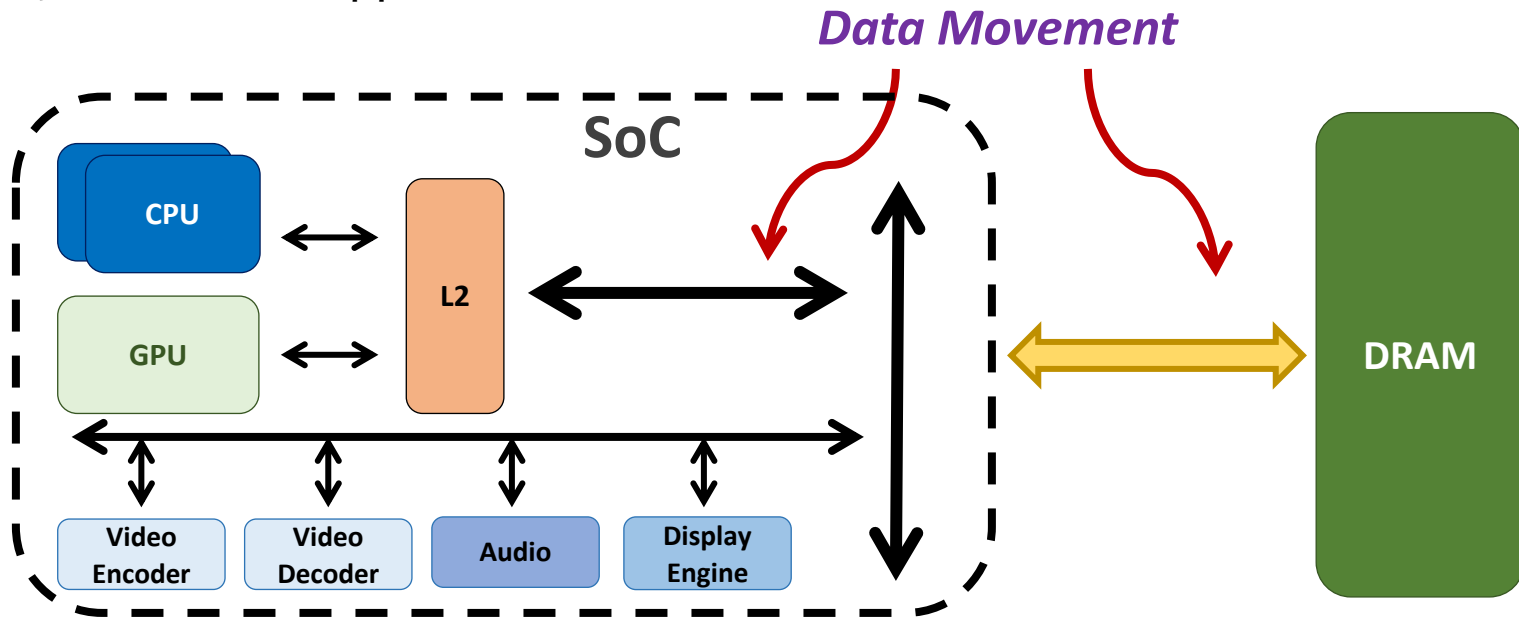


October 29th, 2023

SAFARI

Data Movement in Computing Systems

- Data movement dominates performance and is a major system energy bottleneck
- Total system energy: data movement accounts for
 - 62% in consumer applications*,
 - 40% in scientific applications*,
 - 35% in mobile applications*



* Boroumand et al., "Google Workloads for Consumer Devices: Mitigating Data Movement Bottlenecks," ASPLOS 2018

* Kestor et al., "Quantifying the Energy Cost of Data Movement in Scientific Applications," IISWC 2013

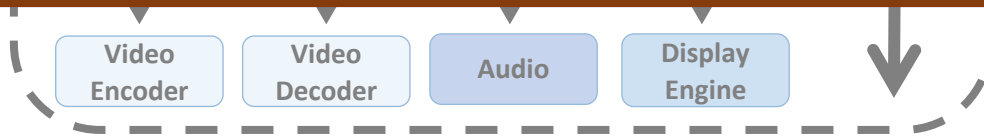
* Pandiyan and Wu, "Quantifying the energy cost of data movement for emerging smart phone workloads on mobile platforms," IISWC 2014

Data Movement in Computing Systems

- Data movement dominates performance and is a major system energy bottleneck
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Compute systems should be more data-centric

Processing-In-Memory proposes computing where it makes sense (where data resides)



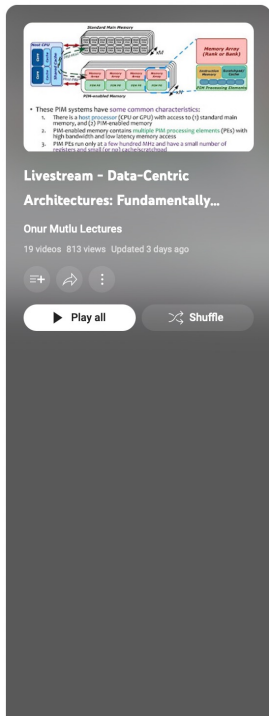
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Processing-in-Memory Course (Spring 2023)

- Short weekly lectures
- Hands-on projects



Livestream - Data-Centric Architectures: Fundamentally...

Onur Mutlu Lectures

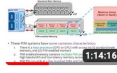
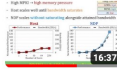

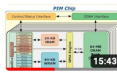
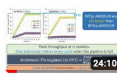




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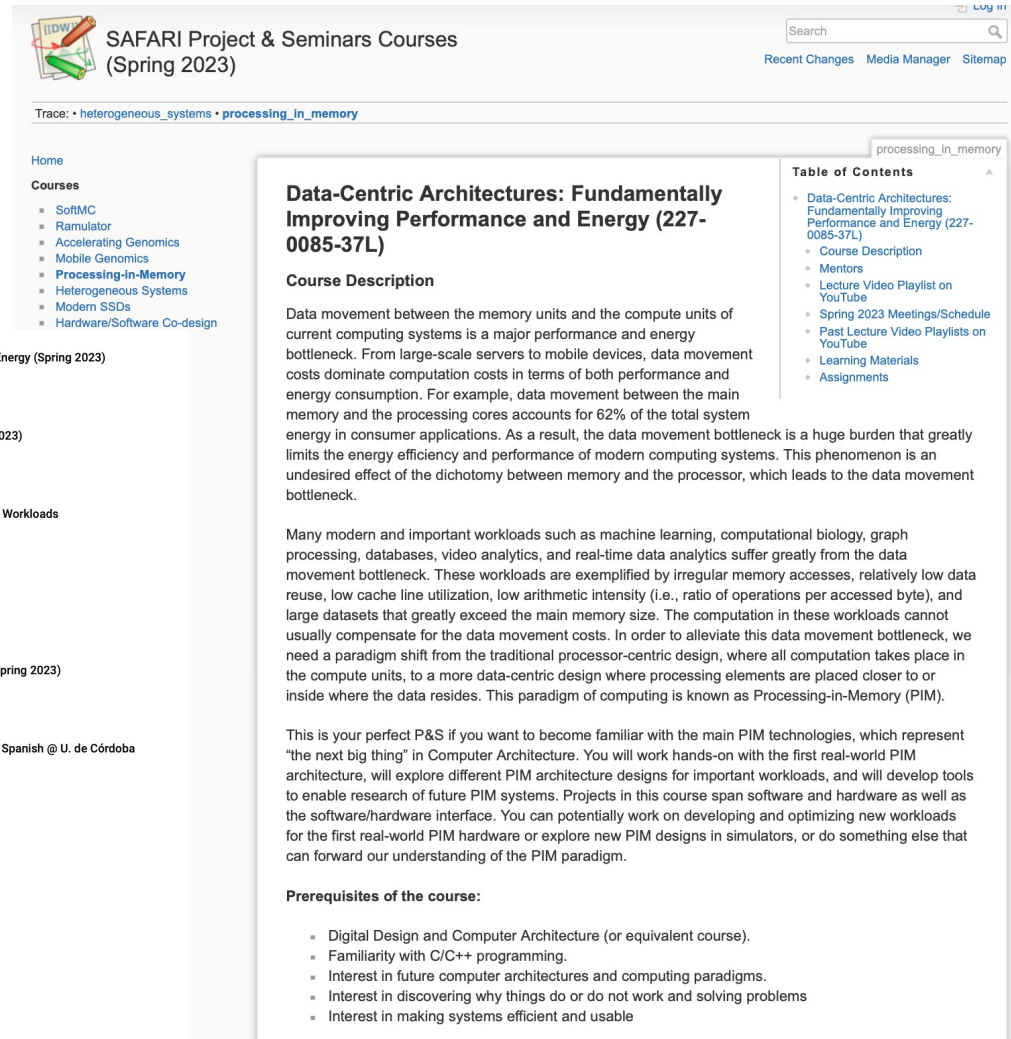
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• These PIM systems have some common characteristics:

1. There is a main processor (CPU or GPU) with access to (1) standard main memory, and (2) PIM enabled memory
2. The enabled memory contains multiple processing elements (PEs) with high bandwidth and low latency memory access
3. The PE usually is a few hundred bits, and has a small number of context and state (one or a few hundred bits)

-  **PIM Course: Lecture 1: Data-Centric Architectures: Improving Performance & Energy (Spring 2023)**
Onur Mutlu Lectures • 1.1K views • Streamed 3 months ago
-  **PIM Course: Lecture 2: How to Evaluate Data Movement Bottlenecks (Spring 2023)**
Onur Mutlu Lectures • 332 views • 2 months ago
-  **ASPLoS 2023 Tutorial: Real-world Processing-in-Memory Systems for Modern Workloads**
Onur Mutlu Lectures • 1.5K views • Streamed 2 months ago
-  **PIM Course: Lecture 3: Real-world PIM: UPMEM PIM (Spring 2023)**
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-  **PIM Course: Lecture 4: Real-world PIM: Microbenchmarking of UPMEM PIM (Spring 2023)**
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-  **Análisis Experimental de una Arquitectura PIM - Juan Gómez Luna - Lecture in Spanish @ U. de Córdoba**
Onur Mutlu Lectures • 169 views • 2 months ago
-  **PIM Course: Lecture 5: Real-world PIM: Samsung HBM-PIM (Spring 2023)**
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-  **PIM Course: Lecture 6: Real-world PIM: SK Hynix AIM (Spring 2023)**
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-  **PIM Course: Lecture 7: Real-world PIM: Samsung AxDIMM (Spring 2023)**
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SAFARI Project & Seminars Courses (Spring 2023)

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- **Processing-in-Memory**
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- Hardware/Software Co-design

processing_in_memory

Data-Centric Architectures: Fundamentally Improving Performance and Energy (227-0085-37L)

Course Description

Data movement between the memory units and the compute units of current computing systems is a major performance and energy bottleneck. From large-scale servers to mobile devices, data movement costs dominate computation costs in terms of both performance and energy consumption. For example, data movement between the main memory and the processing cores accounts for 62% of the total system energy in consumer applications. As a result, the data movement bottleneck is a huge burden that greatly limits the energy efficiency and performance of modern computing systems. This phenomenon is an undesired effect of the dichotomy between memory and the processor, which leads to the data movement bottleneck.

Many modern and important workloads such as machine learning, computational biology, graph processing, databases, video analytics, and real-time data analytics suffer greatly from the data movement bottleneck. These workloads are exemplified by irregular memory accesses, relatively low data reuse, low cache line utilization, low arithmetic intensity (i.e., ratio of operations per accessed byte), and large datasets that greatly exceed the main memory size. The computation in these workloads cannot usually compensate for the data movement costs. In order to alleviate this data movement bottleneck, we need a paradigm shift from the traditional processor-centric design, where all computation takes place in the compute units, to a more data-centric design where processing elements are placed closer to or inside where the data resides. This paradigm of computing is known as Processing-in-Memory (PIM).

This is your perfect P&S if you want to become familiar with the main PIM technologies, which represent "the next big thing" in Computer Architecture. You will work hands-on with the first real-world PIM architecture, will explore different PIM architecture designs for important workloads, and will develop tools to enable research of future PIM systems. Projects in this course span software and hardware as well as the software/hardware interface. You can potentially work on developing and optimizing new workloads for the first real-world PIM hardware or explore new PIM designs in simulators, or do something else that can forward our understanding of the PIM paradigm.

Prerequisites of the course:

- Digital Design and Computer Architecture (or equivalent course).
- Familiarity with C/C++ programming.
- Interest in future computer architectures and computing paradigms.
- Interest in discovering why things do or do not work and solving problems
- Interest in making systems efficient and usable

https://safari.ethz.ch/projects_and_seminars/spring2023/doku.php?id=processing_in_memory

Real PIM Tutorial (HPCA 2023)

- February 26th: Lectures + Hands-on labs + Invited lectures

HPCA 2023 Real-World PIM Tutorial

Real-world Processing-in-Memory Architectures

Tutorial Description

Processing-in-Memory (PIM) is a computing paradigm that aims at overcoming the data movement bottleneck (i.e., the waste of execution cycles and energy resulting from the back-and-forth data movement between memory units and compute units) by making memory compute-capable.

Explored over several decades since the 1960s, PIM systems are becoming a reality with the advent of the first commercial products and prototypes.

A number of startups (e.g., UPMEM, Neuroblade, Mythic) are already commercializing real PIM hardware, each with its own design approach and target applications. Several major vendors (e.g., Samsung, SK Hynix, Alibaba) have presented real PIM chip prototypes in the last two years.

Most of these architectures have in common that they place compute units near the memory arrays. But, there is more to come: Academia and Industry are actively exploring other types of PIM by, e.g., exploiting the analog operation of DRAM, SRAM, flash memory and emerging non-volatile memories.

PIM can provide large improvements in both performance and energy consumption, thereby enabling a commercially viable way of dealing with huge amounts of data that is bottlenecking our computing systems. Yet, it is critical to examine and research adoption issues of PIM using especially learnings from real PIM systems that are available today.

This tutorial focuses on the latest advances in PIM technology. We will (1) provide an introduction to PIM and taxonomy of PIM systems, (2) give an overview and a rigorous analysis of existing real-world PIM hardware, (3) conduct hand-on labs using real PIM systems, and (4) shed light on how to enable the adoption of PIM in future computing systems.

2,560-DPU Processing-in-Memory System

<https://arxiv.org/pdf/2105.03814.pdf>

Goal: Processing Inside Memory

Processor Core

Cache

Memory

Database

Graphs

Media

Query

Results

Interconnect

- Many questions ... How do we design the:
 - compute-capable memory & controllers?
 - processors & communication units?
 - software & hardware interfaces?
 - system software, compilers, languages?
 - algorithms & theoretical foundations?

HPCA 2023 Tutorial: Real-World Processing-in-Memory Architectures

Onur Mutlu Lectures

32.1K subscribers

1.8K views Streamed 1 month ago

Livestream - P&S Data-Centric Architectures: Fundamentally Improving Performance and Energy (Fall 2022)

HPCA 2023 Tutorial: Real-World Processing-in-Memory Architectures

<https://events.safari.ethz.ch/real-pi...>

Time	Speaker	Title	Materials
8:00am-8:40am	Prof. Onur Mutlu	Memory-Centric Computing	(PDF) (PPT)
8:40am-10:00am	Dr. Juan Gómez Luna	Processing-Near-Memory: Real PNM Architectures Programming General-purpose PIM	(PDF) (PPT)
10:20am-11:00am	Dr. Dimin Niu	A 3D Logic-to-DRAM Hybrid Bonding Process-Near-Memory Chip for Recommendation System	
11:00am-11:40am	Dr. Christina Giannoula	SparseP: Towards Efficient Sparse Matrix Vector Multiplication on Real Processing-In-Memory Architectures	(PDF) (PPT)
1:30pm-2:10pm	Dr. Juan Gómez Luna	Processing-Using-Memory: Exploiting the Analog Operational Properties of Memory Components	(PDF) (PPT)
2:10pm-2:50pm	Dr. Manuel Le Gallo	Deep Learning Inference Using Computational Phase-Change Memory	
2:50pm-3:30pm	Dr. Juan Gómez Luna	PIM Adoption Issues: How to Enable PIM Adoption?	(PDF) (PPT)
3:40pm-5:40pm	Dr. Juan Gómez Luna	Hands-on Lab: Programming and Understanding a Real Processing-in-Memory Architecture	(Handout) (PDF) (PPT)

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Real PIM Tutorial (ASPLOS 2023)

- March 26th: Lectures + Hands-on labs + Invited lectures

ASPLOS 2023 Real-World PIM Tutorial

Real-world Processing-in-Memory Systems for Modern Workloads

Important note about registration

Tutorial Description

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2,560-DPU Processing-in-Memory System

PIM can provide large improvements in both performance and energy consumption for many modern applications, thereby enabling a commercially viable way of dealing with huge amounts of data that is bottlenecking our computing systems. Yet, it is critical to (1) study and understand the characteristics that make a workload suitable for a PIM architecture, (2) assess estimation strategies for PIM kernels, and (3)

Tutorial Materials

Time	Speaker	Title	Materials
9:00am-10:20am	Prof. Onur Mutlu	Memory-Centric Computing	PDF PPT
10:40am-12:00pm	Dr. Juan Gómez Luna	Processing-Near-Memory: Real PNM Architectures Programming General-purpose PIM	PDF PPT
1:40pm-2:20pm	Prof. Alexandra (Sasha) Fedorova (UBC)	Processing in Memory in the Wild	PDF PPT
2:20pm-3:20pm	Dr. Juan Gómez Luna & Ataberk Olgun	Processing-Using-Memory: Exploiting the Analog Operational Properties of Memory Components	PDF PPT PDF PPT
3:40pm-4:10pm	Dr. Juan Gómez Luna	Adoption issues: How to enable PIM? Accelerating Modern Workloads on a General-purpose PIM System	PDF PPT PDF PPT
4:10pm-4:50pm	Dr. Yongkee Kwon & Eddy (Chanwook) Park (SK Hynix)	System Architecture and Software Stack for GDDR6-AiM	PDF PPT
4:50pm-5:00pm	Dr. Juan Gómez Luna	Hands-on Lab: Programming and Understanding a Real Processing-in-Memory Architecture	Handout PDF PPT

ASPLOS 2023 Tutorial
Real-world Processing-in-Memory Systems for Modern Workloads

Accelerating Modern Workloads on a General-purpose PIM System

Dr. Juan Gómez Luna
Professor Onur Mutlu

ETH Zürich SAFARI

ASPLOS 2023 Tutorial: Real-world Processing-in-Memory Systems for Modern Workloads
Sunday, March 26, 2023

ASPLOS 2023 Tutorial: Real-world Processing-in-Memory Systems for Modern Workloads

Onur Mutlu Lectures

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Real PIM Tutorial (ISCA 2023)

- June 18th: Lectures + Hands-on labs + Invited lectures

Real-world Processing-in-Memory Systems for Modern Workloads

Tutorial Description

Processing-in-Memory (PIM) is a computing paradigm that aims at overcoming the data movement bottleneck (i.e., the waste of execution cycles and energy resulting from the back-and-forth data movement between memory units and compute units) by making memory compute-capable.

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PIM can provide large improvements in both performance and energy consumption for many modern applications, thereby enabling a commercially viable way of dealing with huge amounts of data that is bottlenecking our computing systems. Yet, it is critical to (1) study and understand the characteristics that make a workload suitable for a PIM architecture, (2) propose optimization strategies for PIM kernels, and (3) develop programming frameworks and tools that can lower the learning curve and ease the adoption of PIM.

This tutorial focuses on the latest advances in PIM technology, workload characterization for PIM, and programming and optimizing PIM kernels. We will (1) provide an introduction to PIM and taxonomy of PIM systems, (2) give an overview and a rigorous analysis of existing real-world PIM hardware, (3) conduct hand-on labs about important workloads (machine learning, sparse linear algebra, bioinformatics, etc.) using real PIM systems, and (4) shed light on how to improve future PIM systems for such workloads.

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 - Agenda (June 18, 2023)
 - Lectures
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10:20am-11:00am	Dr. Juan Gómez Luna	Processing-Near-Memory: Real PNM Architectures / Programming General-purpose PIM	(PDF) (PPT)
11:20am-11:50am	Prof. Izzat El Hajj	High-throughput Sequence Alignment using Real Processing-in-Memory Systems	(PDF) (PPT)
11:50am-12:30pm	Dr. Christina Giannoula	SparseP: Towards Efficient Sparse Matrix Vector Multiplication for Real Processing-In-Memory Systems	(PDF) (PPT)
2:00pm-2:45pm	Dr. Sukhan Lee	Introducing Real-world HBM-PIM Powered System for Memory-bound Applications	(PDF)
2:45pm-3:30pm	Dr. Juan Gómez Luna / Ataberk Olgun	Processing-Using-Memory: Exploiting the Analog Operational Properties of Memory Components / PUM Prototypes: PiDRAM	(PDF) (PPT) (PDF) (PPT)
4:00pm-4:40pm	Dr. Juan Gómez Luna	Accelerating Modern Workloads on a General-purpose PIM System	(PDF) (PPT)
4:40pm-5:20pm	Dr. Juan Gómez Luna	Adoption Issues: How to Enable PIM?	(PDF) (PPT)
5:20pm-5:30pm	Dr. Juan Gómez Luna	Hands-on Lab: Programming and Understanding a Real Processing-in-Memory Architecture	(Handout) (PDF) (PPT)

SAMSUNG

Introducing Real-world HBM-PIM Powered System for Memory-bound Applications

Samsung Electronics
DRAM Design Team
Sukhan Lee

ISCA 2023 Tutorial: Real-world Processing-in-Memory Systems for Modern Workloads

Onur Mutlu Lectures
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<https://events.safari.ethz.ch/isca-pim-tutorial/doku.php?id=start>

Real PIM Tutorial (MICRO 2023)

- October 29th: Lectures + Hands-on labs + Invited lectures



MICRO 2023 Real-World PIM Tutorial

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Real-world Processing-in-Memory Systems for Modern Workloads

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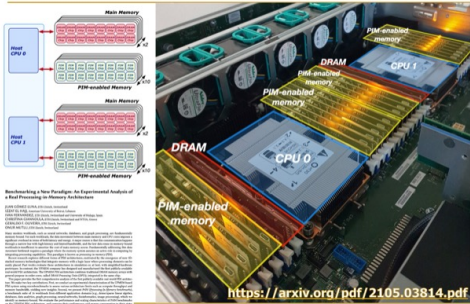
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2,560-DPU Processing-in-Memory System



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Livestream

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Agenda (EDT GMT-4)

- 7:55am-8:00am, Dr Juan Gómez Luna, “Welcome & Agenda.”
- 8:00am-9:20am, Prof. Onur Mutlu / Geraldo F. Oliveira, "Memory-centric Computing: Introduction to PIM as a Paradigm to Overcome the Data Movement Bottleneck."
 - PIM taxonomy: PNM (processing near memory) and PUM (processing using memory).
 - DAMOV Workload Characterization Methodology.
- 9:20am-10:20am, Dr. Juan Gómez Luna, “Processing-Near-Memory: Real PNM.”
 - PNM prototypes: Samsung HBM-PIM, SK Hynix AiM, Samsung AxDIMM, Alibaba HB-PNM.
 - UPMEM PIM: Architecture Characterization, Programming.
- Coffee break (10:20am-10:40am)
- 10:40am-11:20am, Prof. Youngsok Kim (Yonsei University), "PID-Join: A Fast In-Memory Join Algorithm for Commodity PIM-Enabled DIMMs."
- 11:20am-12:00pm, Dr. Abu Sebastian (IBM Research - Zürich), "PUM Based on Memristive Devices: The IBM HERMES Project Chip."
- Lunch break (12:00pm-1:00pm)
- 1:00pm-2:00pm, Geraldo F. Oliveira, "Processing-Using-DRAM: Ambit, SIMDRAM, pLUTo."
- 2:00pm-3:15pm, Dr. Juan Gómez Luna, “Accelerating Modern Workloads on a General-purpose PIM System: Machine learning, Genomics...”
- 3:15pm-3:45pm, Dr. Juan Gómez Luna, “Adoption Issues: How to Enable PIM?”
- 3:45pm-4:15pm, Dr. Juan Gómez Luna, "SimplePIM: A Software Framework for High-level PIM Programming."
- 4:15pm-5:00pm, Ataberk Olgun, "Processing-Using-Memory Prototypes: PiDRAM."
- 5:00pm-5:10pm, Dr. Juan Gómez Luna, “Introduction/Preparation for Hands-on Labs.”
 - Optional - Hands-on Lab: Programming and Understanding a Real PIM Architecture.

Join Algorithm for Commodity PIM DIMMs

- **PID-Join: A Fast In-Memory Join Algorithm for Commodity PIM-Enabled DIMMs**
 - Prof. Youngsok Kim
- **Abstract:** Modern dual in-line memory modules (DIMMs) now allow applications to offload their memory-intensive operations onto the in-DIMM processors (IDPs) located near the memory banks of a DIMM. The IDPs can greatly accelerate in-memory joins whose performance is frequently bottlenecked by main-memory accesses. In this talk, I will present PID-Join, a fast in-memory join algorithm which exploits the IDPs to further improve the performance of in-memory joins. PID-Join is optimized for UPMEM DIMMs, currently the only publicly-available DIMMs equipped with the IDPs. PID-Join achieves significant speedups over the existing CPU-based join implementations by prototyping and evaluating hash, sort-merge, and nested-loop algorithms optimized for the IDPs, enabling fast inter-IDP communication using host CPU cache streaming and vector instructions, and facilitating fast rank-wise data transfers between the IDPs and the main memory.
- **Bio:** [Youngsok Kim](#) is currently an assistant professor with the Department of Computer Science at Yonsei University. His research interests span computer architecture and system software with an emphasis on architecture-conscious database management systems, performance modeling, and architectural support for deep learning. He received his BSc and PhD in Computer Science and Engineering from POSTECH. He was a post-doc researcher at Seoul National University before joining Yonsei University, and was an intern at Consumer Hardware, Google Inc. and S.LSI Business, Samsung Electronics Co., Ltd. during his PhD studies.

PUM based on Memristive Devices

- PUM based on Memristive Devices: The IBM HERMES Project Chip
 - Dr. Abu Sebastian
- **Abstract:** I will introduce analog in-memory computing (or processing using memory) based on memristive technology. A multi-tile, mixed-signal AIMC prototype chip (The IBM HERMES Project Chip) aimed at deep learning inference application will be presented. This chip fabricated in 14nm CMOS technology comprises 64 AIMC cores/tiles based on phase-change memory technology. I will delve deeper into the device, circuits, architectural and algorithmic aspects of AIMC based on this prototype chip. Finally, I will conclude with a brief overview of on-going research activities.
- **Bio:** Dr. Abu Sebastian is one of the technical leaders of IBM's research efforts towards next generation AI Hardware and manages the in-memory computing group at IBM Research - Zurich. He is the author of over 200 publications in peer-reviewed journals/conference proceedings and holds over 90 US patents. In 2015 he was awarded the European Research Council (ERC) consolidator grant and in 2020, he was awarded an ERC Proof-of-concept grant. He was an IBM Master Inventor and was named Principal and Distinguished Research Staff Member in 2018 and 2020, respectively. In 2019, he received the Ovshinsky Lectureship Award for his contributions to "Phase-change materials for cognitive computing". In 2023, he was conferred the title of Visiting Professor in Materials by University of Oxford. He is a distinguished lecturer and fellow of the IEEE. Homepage: <https://research.ibm.com/people/abu-sebastian>

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